

WE CLAIM:

1. A method for forming an integrated circuit structure, comprising the steps of:
  - 5 providing a substrate having a semiconductor surface;
  - forming an oxygen-containing layer on said semiconductor surface;
  - 10 forming a uniform nitrogen distribution throughout said oxygen-containing layer; and
  - 15 re-oxidizing said layer by a rapid anneal step in an oxidizer and hydrogen mixture of N<sub>2</sub>O and H<sub>2</sub> for stabilizing the nitrogen distribution at minimum oxidation rate, healing plasma-induced damage and reducing interfacial defect density.
2. The method according to Claim 1 wherein said oxygen-containing layer is an ultra-thin silicon dioxide layer in the thickness range from 0.6 to 2.0 nm.
3. The method according to Claim 1 wherein said oxygen-containing layer is an oxynitride layer.
- 20 4. The method according to Claim 1 wherein said step of forming an oxide is a rapid thermal oxidation.
5. The method according to Claim 1 wherein said anneal steps comprise 5 to 60 s at 800 to 1050 °C in N<sub>2</sub>O/H<sub>2</sub>,  
25 flowing at 1 to 20 standard liters/min at 2 to 50 Torr.
6. The method according to Claim 5 wherein said N<sub>2</sub>O/H<sub>2</sub> mixture contains 0.5 to 30 % (preferred 1 %) H<sub>2</sub> with the balance N<sub>2</sub>O.
7. The method according to Claim 1 wherein said oxidizer and hydrogen mixture comprises NO and H<sub>2</sub>, or O<sub>2</sub> and H<sub>2</sub>.
- 30 8. The method according to Claim 1 wherein said reduced

interface state density provides higher carrier mobility in the channel of said transistor.

9. The method according to Claim 1 wherein said integrated circuit structure includes a transistor having a conductive gate structure disposed on a gate dielectric layer;

wherein said dielectric layer, after annealing and re-oxidizing, forms said gate dielectric layer; and further comprising the step of:

10 forming said conductive gate structure upon said gate dielectric layer.

11. The method according to Claim 9 wherein said conductive gate is comprised of doped poly-silicon.

12. The method according to Claim 9 wherein said gate dielectric is an ultra-thin silicon dioxide layer.

13. The method according to Claim 9 further comprising the steps of forming source and drain and their respective contact to complete said transistor.

14. The method according to Claim 1 wherein said integrated circuit structure includes a capacitor having a capacitor dielectric; and further comprising the steps of:

20 forming a first electrode over said substrate, said semiconductor surface present at said first electrode; and

25 forming a second electrode on said dielectric layer; wherein said dielectric layer forms said capacitor dielectric.

30 15. An integrated circuit having a component as produced by the method of Claim 1.

16. The circuit according to Claim 14 wherein said component is a transistor.

16. The circuit according to Claim 14 wherein said component is a capacitor.

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